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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/721,382	11/26/2003	Hien Boon Tan	Q78432	6007
23373 7590 10/10/2008				
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SUITE 800				
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EXAMINER				
GRAYBILL, DAVID E				
ART UNIT		PAPER NUMBER		
2894				
MAIL DATE		DELIVERY MODE		
10/10/2008		PAPER		

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/721,382

Applicant(s)

TAN ET AL.

Examiner

David E. Graybill

Art Unit

2894

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 19 June 2008.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 25-27 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 25-27 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-946)
- 3) ☐ Information Disclosure Statement(s) (PTO/SE/US)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 25-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Yee (6825062) and Minamio (6710430).

At column 7, line 14 to column 8, line 37; column 9, lines 18-56; and column 11, line 48 to column 13, lines 29-53; and column 13, line 59 to column 14, line 20, Yee discloses the following:

Re claim 25: A method of assembling an integrated circuit package, comprising:
a) providing: a leadframe 10 having a first face and a second face opposite to said first face, wherein said leadframe comprises: an outer frame portion 18, a die pad portion 16 substantially centrally disposed within said outer frame portion, a plurality of tie bars connecting said die pad portion to said outer frame portion, and a plurality of

protuberances 11 extending substantially radially inward from said outer frame portion, each of said plurality of protuberances comprising an inner lead portion (illustrated in Fig. 3D directly bonded to 3), an outer lead portion (illustrated in Fig. 3D rightwardly adjacent to 14), and a post portion connecting said inner lead portion from said outer lead portion, an integrated circuit chip 2 having a first face and a second face opposite to said first face, a first plurality of wires 3 each having a first end and a second end, and a second plurality of wires 3 each having a first end and a second end; b) disposing an adhesive layer 32 on said first face of said leadframe, whereby said adhesive layer covers said die pad portion, and part of said inner lead portion of each of said plurality of protuberances, wherein part of each of said inner lead portions remains free of adhesive; d) mounting said integrated circuit chip on said leadframe, whereby said second face of said integrated circuit chip is connected to a first face of said die pad portion through said adhesive layer, and whereby said second face of said integrated circuit is further connected to said inner lead portions through said adhesive layer; e) electrically conductively joining said first end of said first plurality of wires to said first face of one of said plurality of inner lead portions; f) electrically conductively joining said second end of each of said first plurality of wires to said first face of said integrated circuit chip; g) electrically conductively joining said first end of each of said second plurality of wires to said first face of one of said lead portions, and h) electrically conductively joining said second end of said second plurality of wires to said first face of said integrated circuit chip.

Re claim 26: The method according to claim 25, wherein the adhesive layer disposed on said first face of said lead frame in step (b) covers an outer edge of said die pad portion, and part of said inner lead portion of each of said plurality of protuberances, thereby leaving a part of each of said inner lead portions remains free of adhesive.

Re claim 27: A method of assembling an integrated circuit package, comprising: providing: a leadframe having a first face and a second face opposite to said first face, wherein said leadframe comprises: an outer frame portion, a die pad portion substantially centrally disposed within said outer frame portion, a plurality of tie bars connecting said die pad portion to said outer frame portion, and a plurality of protuberances extending from said leadframe, wherein some of said protuberances comprise at least a plurality of inner lead portions and some of said protuberances comprise at least a plurality of outer lead portions; an integrated circuit chip having a first face and a second face opposite to said first face, a first plurality of wires each having a first end and a second end, and a second plurality of wires each having a first end and a second end; b) disposing an adhesive layer on said first face of said leadframe, whereby said adhesive layer covers said die pad portion, and part of said inner lead portions, wherein part of each of said inner lead portions remains free of adhesive; c) mounting said integrated circuit chip on said leadframe, whereby said second face of said integrated circuit chip is connected to a first face of said die pad portion through said adhesive layer, and whereby said second face of said integrated circuit is further connected to said inner lead portions through said adhesive layer; d)

electrically conductively joining said first end of said first plurality of wires to said first face of one of said plurality of inner lead portions; e) electrically conductively joining said second end of each of said first plurality of wires to said first face of said integrated circuit chip; f) electrically conductively joining said first end of each of said second plurality of wires to said first face of one of said lead portions, and g) electrically conductively joining said second end of said second plurality of wires to said first face of said integrated circuit chip.

To further clarify the disclosure of a post portion, Yee discloses, "FIG. 3B illustrates a case in which two dimples are formed at opposite sides of the each inner lead 12, respectively, in such a fashion that each of them extends partially over an associated peripheral edge of the inner lead 12 and an associated side surface of the inner lead 12." In addition, Yee discloses, "FIG. 3D is a cross-sectional view partially illustrating a semiconductor package 1 fabricated using a lead frame (not shown) provided with at least one aperture, in place of the dimple, as the lead lock 14 for each lead." Therefore, the inner lead portion directly between the dimples/apertures is a post portion.

To further clarify, Yee explicitly discloses any combination of explicitly disclosed embodiments relied on supra because Yee discloses the following:

The lead frames shown in FIGS. 1 to 6B can be advantageously used to fabricate bottom lead type semiconductor packages in which the entire lower surface of each inner lead 12 is exposed at the bottom of the resin encapsulate 4, as shown in FIGS. 3C, 3D, 4, 5E, 6A, and 6B, or lead end grid type semiconductor packages in which only the lower surface of the protruded end 19 protruded from the lower surface of each inner lead 12 is exposed at the bottom of the resin encapsulate 4, as shown in FIGS. 7A to 7D.

Furthermore, 37 CFR 1.84(p)(4) states:

The same part of an invention appearing in more than one view of the drawing must always be designated by the same reference character, and the same reference character must never be used to designate different parts.

Therefore, reference character 1 designates the same part throughout the figures.

In any case, it would have been obvious to combine the embodiments of Yee because Yee discloses that they are drawn to the same invention for the same purpose.

However, Yee does not appear to explicitly disclose the following:

Re claim 26: wherein the adhesive layer disposed on said first face of said lead frame in step (b) covers only an outer edge of said die pad portion, thereby leaving a central part of said die pad portion free of adhesive.

Regardless, in the instant claims, the omission of the element of Yee wherein the adhesive layer disposed on said first face of said lead frame in step (b) covers a central part of said die pad portion is obvious because omission of a step or an element and its function is obvious if the function of the element is not desired or required. See *Ex parte Wu*, 10 USPQ 2031 (Bd. Pat. App. & Inter. 1989); *In re Larson*, 340 F.2d 965, 144 USPQ 347 (CCPA 1965); *In re Kuhle*, 526 F.2d 553, 188 USPQ 7 (CCPA 1975); and MPEP 2144.04IIA.

Also, Yee does not appear to explicitly disclose the following:

Re claim 25: c) severing said outer lead portion from said inner lead portion by cutting said post portion.

Re claim 27: f) electrically conductively joining said first end of each of said second plurality of wires to said first face of one of said outer lead portions.

Nevertheless, at column 4, lines 58-67; column 8, lines 7-52; column 13, lines 18-39 and 41-48; and column 15, lines 12-22, Minamio discloses severing outer lead portion 14 from inner lead portion 16 by cutting a post portion 17, and electrically conductively joining a first end of each of a second plurality of wires 21 to a first face of one of the outer lead portions.

Moreover, it would have been obvious to combine this disclosure of Minamio with the disclosure of Yee because, as disclosed by Minamio, "it is possible to easily obtain a semiconductor device having three or more rows of external terminals; and, as disclosed by Yee as cited, the lead frames of Yee "can be advantageously used" to fabricate bottom lead type semiconductor packages such as the package of Minamio.

Applicant's amendment and remarks filed 9-28-7 have been fully considered and are adequately treated supra.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the

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advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

For information on the status of this application applicant should check PAIR:

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Alternatively, applicant may contact the File Information Unit at (703) 308-2733. Telephone status inquiries should not be directed to the examiner. See MPEP 1730VIC, MPEP 203.08 and MPEP 102.

Any other telephone inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Graybill at (571) 272-1930. Regular office hours: Monday through Friday, 8:30 a.m. to 6:00 p.m.
The fax phone number for group 2800 is (571) 273-8300.

/David E Graybill/
Primary Examiner, Art Unit 2894